Listing of the Claims

1. (Previously Presented) A method for controlling virtual memory address translation during data movement operations enabled in a hardware environment, comprising the steps of:

monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory; and

upon detection of a TLB purge prior to completion of the data movement operation, aborting the data movement operation pending reestablishment of accurate virtual-memory-to-physical-memory mapping.

2. (Original) The method of claim 1, further comprising the step of enqueuing status information on whether the data movement operation completed or was aborted.

3. (Original) The method of claim 2, in which said status information includes identification of data that was successfully moved prior to an abort.

4. (Original) The method of claim 1, in which the data movement operation is a data copying operation.

5. (Previously Presented) A method for controlling virtual memory address translation during data movement operations enabled in a hardware environment, comprising the steps of:

monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory;

upon detection of a TLB purge prior to completion of the data movement operation, aborting the data movement operation pending reestablishment of accurate virtual-memory-to-physical-memory mapping; and

enqueuing status information on whether the data movement operation completed or was aborted.

6. (Previously Presented) Hardware for controlling virtual memory address translation during data operations involving physical movement of data, the hardware comprising:

means for setting a first flag upon initiation of a data operation;

means for periodically monitoring for translation lookaside buffer (TLB) purges;

means for translating virtual address space to physical address space;

means for setting up one or more input registers on a data mover;

means, responsive to said means for translating and said means for setting up, for clearing the first flag if a TLB purge has been detected; and

means for aborting the data operation and then enqueuing a first operation completion status if a TLB purge is detected before physical movement of data is complete.

7. (Previously Presented) The hardware of claim 17, in which the second operation completion status indicates completion of the data operation.

8. (Previously Presented) The hardware of claim 6, in which the first operation completion status identifies data that was successfully moved prior to the abort.

9. (Previously Presented) The hardware of claim 6, in which the data operation is a data copying operation.

10. (Previously Presented) The hardware of claim 16, in which the means for clearing the first flag and setting a second flag is enabled if a TLB purge has not been detected before physical data movement is to commence.

11. (Previously Presented) The hardware of claim 6, in which the means for clearing the first flag is enabled if a TLB purge has been detected before physical data.

12. (Previously Presented) The method of claim 1, wherein said occurrence of a TLB purge is indicative that a change in virtual-memory-to-physical-memory mapping has occurred.

13. (Previously Presented) The method of claim 5, wherein said occurrence of a TLB purge is indicative that a change in virtual-memory-to-physical-memory mapping has occurred.

14. (Previously Presented) The method of claim 5 further comprising:

enqueuing status information including identification of data that was successfully moved prior to the abort.

15. (Previously Presented) The hardware of claim 6, wherein an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory is indicative that a change in virtual-memory-to-physical-memory mapping has occurred.

16. (Previously Presented) The hardware of claim 6 further comprising:

means, responsive to said means for translating and said means for setting up, for clearing the first flag and setting a second flag if a TLB purge has not been detected;

means for examining the second flag; and

means for commencing physical movement of data if the second flag is set;

17. (Previously Presented) The hardware of claim 6 further comprising:

means for enqueuing a second operation completion status if a TLB purge is not detected before physical movement of data is complete.